AF/1770

TRANSMITTAL FORM

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Application No.	10/676,666
Filing Date	September 30, 2003
First Named Inventor	Randy B. Osborne
Art Unit	2816
Examiner Name	Paul W. Schlie
Total Number of Pages in This Submission	
Attorney Docket Number	42P16964

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Gregory D. Caldwell, Reg. No. 39,926 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	June 30, 2006

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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

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Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($) 500.00

SUBMITTED BY *Complete (if applicable)*

Name (Print/Type)	Gregory D. Caldwell	Registration No. (Attorney/Agent)	39,926	Telephone	(503) 439-8778
Signature				Date	06/30/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Randy B Osborne et al

Serial No.: 10/676,666 Group Art Unit: 2186

Filed: September 30, 2003 Examiner: Schlie, Paul W

FOR: METHOD AND APPARATUS FOR SELECTIVE DRAM PRECHARGE

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On: June 30, 2006

Signature: Katherine Jennings

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
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Sir:

Applicant (hereinafter Appellant) submits this appeal brief, thus perfecting the notice of appeal filed on May 3, 2006.

The required headings and subject matter follow.

(i) Real party in interest.

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) Related appeals and interferences.

There are no known related appeals and / or interferences.

(iii) Status of claims.

Claims 1-15 are pending in the case and stand rejected. The rejections of claims 1-15 are being appealed.

(iv) Status of amendments.

No amendments were filed subsequent to the final rejection.

(v) Summary of claimed subject matter.

Paragraph numbering of the filed application and the published application may differ. Accordingly, the following description references paragraphs of the present application based upon the paragraph numbering of the application as published on March 31, 2005. Further, supplied reference numbers and paragraphs are not meant to limit the scope of the present claims but merely to provide examples of some elements to aid understanding. The actually claim scope may be broader and/or more narrow than the example elements given.

Claim 1 is directed to an apparatus comprising a plurality of banks such as 199a-199d, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein only one row of memory cells in each bank may be activated to be open to be accessed at any given time; control logic 191 coupled to the plurality of banks to control accesses made to each bank in response to commands received from an external device including a precharge command wherein banks of the plurality of banks that are affected by the precharge command are individually specified; and a plurality of signal lines coupling the control logic to the external device able to support the precharge command using individual ones of a subset of the plurality

of signal lines to individually specify the banks of the plurality of banks that are affected by the precharge command.

Claim 6 is directed to a computer system comprising a CPU 410; a memory device 490 having a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein the memory device is capable of closing open rows in banks individually specified in a precharge command; a memory bus comprised of a plurality of signal lines coupled to the memory device; and a memory controller 470 coupled to the CPU 410 and to the memory bus to transmit the precharge command to the memory device 490 across the memory bus wherein banks within the memory device 490 having an open row to be closed in response to the precharge command are individually specified through corresponding individual ones of a subset of the plurality of signal lines of the memory bus.

Claim 9 is directed to a method comprising determining whether or not there is a bank within a plurality of banks within a memory device 190 having an open row that must be closed in preparation for an upcoming access command; and transmitting a precharge command to the memory device 190 through a subset of signal lines of a memory bus comprised of a plurality of signal lines using individual ones of the subset of signal lines to individually specify at least one bank within the memory device 190 having an open row that is to be closed.

Claim 14 relates to a machine-accessible medium such as a the storage media 461 and/or non-volatile memory device 430 comprising code that when executed by a processor such as the CPU 410 within an electronic device 400, causes the electronic device 400 to carry out a test of a memory device 490 to determine whether or not the memory device 490 supports a precharge command in which individual ones of a subset of signal lines of a memory bus comprised of a plurality of signal lines are used to individually specify at least one of a plurality of banks

comprising the memory device 490 having an open row of memory cells that is to be closed; and program a memory controller 470 coupling the memory device 490 to the CPU 410 to enable the use of a precharge command in which individual ones of the subset of signal lines are used to individually specify at least one of the plurality of banks as an alternative to using a plurality of bank address lines to transmit a binary code across the memory bus specifying only one bank of the plurality of banks having an open row of memory cells that is to be closed in an alternate form of precharge command.

(vi) Grounds of rejection to be reviewed on appeal.

Whether claims 14-15 fail to comply with the enablement requirement under 35 U.S.C. § 112 first paragraph.

Whether claims 1-5 are unpatentable under 35 U.S.C. § 103(a) over Watanbe (5, 463, 590) in further view of Osborne (US Application 10/676,666).

Whether claims 6-9 and 11-13 are unpatentable under 35 U.S.C. § 103(a) over Watanbe (5, 463, 590) and Osborne (US Application 10/676,666) in further view of "NEC Preliminary User's manual, memory controller NA85E35, NBA85E535Vxx" (NEC Manual, hereafter), second edition, as published 10/2002 in English and 8/2002 in Japanese.

Whether claim 10 is unpatentable under 35 U.S.C. § 103(a) over Watanbe (5, 463, 590) and Osborne (US Application 10/676,666) and NEC Manual in further view of Rovati (6, 182, 192).

Whether claims 14-15 are unpatentable under 35 U.S.C. § 103(a) over Watanbe (5, 463, 590) and Osborne (US Application 10/676,666) and NEC Manual in further view of Shaver (5, 974, 501).

(vii) Argument.

Claim Rejections under 35 USC § 112 first Paragraph

The rejection of claims 14-15 under 35 U.S.C. §112 first paragraph, as failing to comply with the enablement requirement is in error and should be reversed.

As is well-established, in order to successfully establish lack of enablement requirement under the first paragraph of 35 U.S.C 112 (see 2106.01, III. Enablement), the office action must establish that there is a *reasonable basis* for questioning the adequacy of the disclosure to enable a person of ordinary skill in the art to make and use the claimed invention without resorting to *undue experimentation.* Therefore, if the claims disclose the invention to an extent that a person of ordinary skill in the art can use the claimed invention without resorting to undue experimentation, the Official Action has not succeeded in questioning the adequacy of the disclosure on reasonable basis.

Claim 14

Claim 14 requires a machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to: carry out a test to determine whether or not the memory device supports a precharge command in which individual ones of a subset of signal lines of a memory bus comprised of a plurality of signal lines are used to individually specify at least one of a plurality of banks comprising the memory device having an open row of memory cells that is to be closed; and program a memory controller coupling the memory device to the CPU to enable the use of a precharge command in which individual ones of the subset of signal lines are used to individually specify at least one of the plurality of banks as an alternative to using a plurality of bank address lines to transmit a binary code across the

memory bus specifying only one bank of the plurality of banks having an open row of memory cells that is to be closed in an alternate form of precharge command.

The final office action appears to indicate that the method to carry out the test to determine whether or not the memory device supports a particular set of attributes is not sufficiently described in the specification. However, the claim clearly indicates the *functions that the test is supposed to perform.* The test that need to be performed to determine the type and the functions supported by the memory device are implementation specific. Given a specific implementation, one skilled in the art may easily determine and perform the tests required to determine the type and functions of the memory device. As a result, a person of ordinary skill in the art may develop a code for such software to perform a test, which determines whether or not the memory device supports the particular set of attributes listed out in claim 14, without undue experimentation. The final official action does not establish that there is a *reasonable basis* for questioning the adequacy of the disclosure to enable a person of ordinary skill in the art to make and use the claimed invention without resorting to *undue experimentation.* Appellant respectfully request that rejection of claim 14 be reversed.

Claim 15

Claim 15 comprise claim 14 as the base claim. Accordingly, claim 15 is allowable for at least the reasons given above. Appellant respectfully requests that the rejection of claim 15 be withdrawn.

Claim Rejections under 35 USC § 103(a) (Watanbe/Osborne)

The rejection of claims 1-5 under 35 U.S.C. §103(a) as being unpatentable under 35 U.S.C. § 103(a) over Watanbe (5, 463, 590) in further view of Osborne (US Application 10/676,666) is in error and should be reversed.

Claim 1

Claim 1 is directed to an apparatus comprising a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein only one row of memory cells in each bank may be activated to be open to be accessed at any given time; control logic coupled to the plurality of banks to control accesses made to each bank in response to commands received from an external device including a precharge command wherein ***banks*** of the plurality of banks ***that are affected by the precharge command are individually specified***; and a plurality of signal lines coupling the control logic to the external device able to support the precharge command using individual ones of a subset of the plurality of signal lines to individually specify the banks of the plurality of banks that are affected by the precharge command.

Osborne (10/676,666) is the instant application and the final office action rejected the claim 1 of the instant application as being unpatentable over Watanbe in view of Osborne. Appellant respectfully indicates that the teachings of Osborne cannot be used as a prior art. Osborne indicates (in paragraph [0002]), that multiple functions may be multiplexed onto various signal inputs and outputs to reduce both cost and physical size of DRAMs. Osborne merely indicates, in the background sections (paragraph [0002]) of the instant application, that multiplexing signal lines can offer some advantages such as cost and space reduction. Osborne does not disclose any details of how the signal lines are multiplexed.

Osborne indicates (in paragraph [0026]), as an example, that address lines A0-A3 in embodiments depicted in Fig. 2a and 2c or the address lines A0-A11 and BA0-BA3 used in the embodiments of Fig. 2b is used ***to individually specify the banks affected by the pre-charge command***. Further, Osborne indicates that one of ordinary skill in the art will readily recognize

that any combination of the address signal lines or other signal lines (perhaps control lines) may be employed for the purpose of ***specifying bank(s) affected by a given precharge command*** and/or providing interoperability with existing DDR variants without deviating from the scope and spirit of the present invention. Osborne merely describes *alternative* embodiments of the present invention that one of ordinary skill in the art may implement in light of the teachings of the instant application.

Also, the final office action appears to rely on claims 1-4 of the Watanbe for teaching individually specifying the banks affected by the pre-charge command. Claim 1 of Watanbe discloses a pre-charging means for pre-charging data lines connected to the memory cells to be read and a plurality of address latch sections each provided for each bank, each for latching addresses of the memory cells to be read, written and refreshed, each of said address latch sections being set to latch status when said bank is activated and to a latch release status when the said bank is pre-charged. Watanbe appears to suggest a memory architecture comprising an address latch whose status is changed based on whether the bank is activated or whether the bank is pre-charged. However, claim 1 does not appear to disclose ***individually specifying the banks affected by the pre-charge command.***

Watanbe discloses (in col. 1, lines 60-64) a DRAM suitable for use with a computer system provided with a high speed CPU, which can increase the operating speed of the memory device without complicating the control system thereof. The DRAM of Watanbe comprises (as described in col. 2 lines 50-52) an all-bank pre-charge means for outputting an all-bank pre-charge signal for pre-charging all the banks forcedly to said pre-charge means and does not teach ***individually specify the banks affected by the pre-charge command*** as required by claim 1 of the instant application. Watanbe discloses, in col. 13, lines 16-19, different signals generated by

the bank activating/deactivating circuit, a bank precharge gating circuit, and a bank activate circuit. However, none of the above referenced sections, or circuits, or the signals generated by these circuits discloses ***individually specifying the banks affected by the pre-charge command*** as required by claim 1 of the instant application. Thus, it would not be obvious to one of ordinary skill in the art to arrive at the invention claimed in claim 1 of the instant application. Appellant respectfully request the rejection of claim 1 be withdrawn.

Claims 2-5

Claims 2-5 comprise claim 1 as the base claim. Accordingly, claims 2-5 is allowable for at least the reasons given above. Appellant respectfully requests that the rejection of claims 2-5 be withdrawn.

Claim Rejections – 35 USC § 103 (Watanbe/Osborne/NEC Manual)

The rejection of claims 6-9 and 11-13 under 35 U.S.C. §103(a) as being unpatentable under 35 U.S.C. § 103(a) over Watanbe (5, 463, 590) and Osborne (US Application 10/676,666) in further view of "NEC Preliminary User's manual, memory controller NA85E35, NBA85E535Vxx" (NEC Manual, hereafter), second edition, as published 10/2002 in English and 8/2002 in Japanese is in error and should be reversed.

Claim 6

Claim 6 is directed to a computer system comprising a CPU; a memory device having a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein the memory device is capable of closing open rows in banks individually specified in a precharge command; a memory bus comprised of a plurality of signal lines coupled to the memory device; and a memory controller coupled to the CPU and to the

memory bus to transmit the precharge command to the memory device across the memory bus wherein banks within the memory device having ***an open row to be closed in response to the precharge command are individually specified*** through corresponding individual ones of a subset of the plurality of signal lines of the memory bus.

Osborne (10/676,666) is the instant application and the claim 6 of the instant application is rejected as being unpatentable over Watanbe in view of Osborne in further view of the NEC manual. Appellant respectfully indicates that the teachings of Osborne cannot be used as a prior art. Watanbe, as described above, discloses a DRAM suitable for use with a computer system provided with a high speed CPU, which can increase the operating speed of the memory device without complicating the control system thereof and does not teach of ***individually specifying the banks affected by the pre-charge command.***

The final office action appears to rely on description in pages 22-25 of the NEC manual to teach a memory controller coupled to a memory device that transmits a pre-charge command, wherein banks within the memory device have ***an open row to be closed in response to the precharge command are individually specified*** through corresponding individual ones of a subset of the plurality of signal lines of the memory bus. The description on pages 22-25 of the NEC manual discloses a memory controller accessing the SDRAM. The status transition of SDRAM access depicted in Fig 1-2 indicates an order or a sequence in which the pre-charge, active, and read/write commands are issued under different conditions. The description on page 22 of NEC Manual indicates the sequence as (i) an all-bank pre-charge command is always issued to the SDRAM after power application and bus hold or during refresh and when accessing SDRAM after the all-bank precharge command, an active command and then a read/write command is issued in that order; (ii) if a page is changed a pre-charge command, an active

command, and a read/write command is issued in that order; and (iii) if the bank is changed, an active command and a read/write command is issued in that order to the bank to be accessed next and a pre-charge command is issued to a bank accessed immediately before the bank that is currently being accessed, immediately after the read/write command is issued.

The NEC manual simply discloses an order or a sequence in which the commands are issued to the SDRAM during start-up, while changing the page, and while changing the bank. However, the NEC manual does not appear to disclose a memory controller transmitting a pre-charge command to the memory device, wherein banks within the memory device have ***an open row to be closed in response to the precharge command are individually specified*** through corresponding individual ones of a subset of the plurality of signal lines of the memory bus as required by claim 6 of the instant application. Thus, it would not be obvious to one skilled in the art to arrive at the invention claimed in claim 6 of the instant application after having teachings of Watanbe and the NEC manual. Appellant respectfully request the rejection of claim 6 be withdrawn.

Claims 7-8

Claims 7-8 comprise claim 6 as the base claim. Accordingly, claims 7-8 is allowable for at least the reasons given above. Appellant respectfully requests that the rejection of claims 7-8 be withdrawn.

Claim 9

Claim 9 is directed to a method comprising determining whether or not there is a bank within a plurality of banks within a memory device ***having an open row that must be closed in preparation for an upcoming access command***; and transmitting a precharge command to the

memory device through a subset of signal lines of a memory bus comprised of a plurality of signal lines ***using individual ones of the subset of signal lines to individually specify at least one bank within the memory device having an open row that is to be closed.***

Claim 9 of the instant application is rejected as being unpatentable over Watanbe in view of Osborne in further view of the NEC manual. Osborne (10/676,666) is the instant application. Appellant respectfully indicates that the teachings of Osborne cannot be used as a prior art. Watanbe, as described above, discloses a DRAM suitable for use with a computer system provided high speed CPU, which can increase the operating speed of the memory device without complicating the control system thereof and does not teach of ***using individual ones of the subset of signal lines to individually specify at least one bank within the memory device having an open row that is to be closed.***

The final office action appears to rely on description in pages 22-25 of the NEC manual to teach a method by which a memory controller coupled to a memory device determines whether or not there is a bank within a plurality of banks within a memory device ***having an open row that must be closed in preparation for an upcoming access command***; and transmits a precharge command to the memory device through a subset of signal lines of a memory bus comprised of a plurality of signal lines ***using individual ones of the subset of signal lines to individually specify at least one bank within the memory device having an open row that is to be closed.***

As described above, the NEC manual simply discloses an order in which the commands are issued to the SDRAM during start-up, while changing the page, and while changing the bank. However, the NEC manual does not appear to disclose a memory controller transmits a precharge command to the memory device through a subset of signal lines of a memory bus

comprised of a plurality of signal lines ***using individual ones of the subset of signal lines to individually specify at least one bank within the memory device having an open row that is to be closed*** as required by claim 9 of the instant application. Thus, it would not be obvious to one skilled in the art to arrive at the invention claimed in claim 9 of the instant application after having teachings of the Watanbe patent and the NEC manual. Appellant respectfully request the rejection of claim 9 be withdrawn.

Claims 11-13

Claims 11-13 comprise claim 9 as the base claim. Accordingly, claims 11-13 is allowable for at least the reasons given above. Appellant respectfully requests that the rejection of claims 11-13 be withdrawn.

Claim Rejections – 35 USC § 103 (Watanbe/Osborne/NEC Manual/Rovati)

The rejection of claim10 under 35 U.S.C. §103(a) as being unpatentable under 35 U.S.C. § 103(a) over Watanbe (5, 463, 590) and Osborne (US Application 10/676,666) and NEC Manual in further view of Rovati (6, 182, 192) is in error and should be reversed.

Claim 10

Claim 10 depends from claim 9 and is allowable for at least the reasons noted above in reference to claim 9. Appellant respectfully request allowance of claim 10.

Claim Rejections – 35 USC § 103 (Watanbe/Osborne/NEC Manual/Shaver)

The Official Action further rejected claims 14-15 under 35 USC 103(a) as being unpatentable over Watanbe (US 5,463,590), Osborne (10/676,666), NEC Manual, in further view of Shaver (US 5,974,501). Applicants respectfully request allowance of claims 14-15 in light of the points that follow.

Claim 14

Claim 14 requires a machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to: carry out a test to determine whether or not the memory device supports a precharge command in which individual ones of a subset of signal lines of a memory bus comprised of a plurality of signal lines are used ***to individually specify at least one of a plurality of banks comprising the memory device having an open row of memory cells that is to be closed***; and program a memory controller coupling the memory device to the CPU to enable the use of a precharge command in which individual ones of the subset of signal lines are used ***to individually specify at least one of the plurality of banks*** as an alternative to using a plurality of bank address lines to transmit a binary code across the memory bus specifying only one bank of the plurality of banks having an open row of memory cells that is to be closed in an alternate form of precharge command.

As described above, Osborne (10/676,666) simply identifies that there may be other alternatives that can be recognized in light of the teachings of the instant application. Further, Osborne cannot be used as a prior art for the reasons noted above. Watanbe, as described above, discloses a DRAM suitable for use with a computer system provided with a high speed CPU, which can increase the operating speed of the memory device without complicating the control system thereof and does not teach of ***individually specifying at least one of a plurality of banks comprising the memory device having an open row of memory cells that is to be closed.*** The NEC manual simply discloses an order in which the commands are issued to the SDRAM during start-up, while changing the page, and while changing the bank. Thus, Watanbe and NEC manual, individually or together, do not teach the invention covered by the scope of claims 14-15 of the instant application.

Further, the final office action appears to rely on Fig. 6 and description in col. 1, lines 1-2 of Shaver for teaching to carry out a test to determine whether or not the memory device supports a precharge command in which individual ones of a subset of signal lines of a memory bus comprised of a plurality of signal lines are used ***to individually specify at least one of a plurality of banks comprising the memory device having an open row of memory cells that is to be closed***. However, Fig. 6 of Shaver discloses a circuitry used to provide memory timing information and addresses for a particular memory cycle in the memory controller. The description in col. 1 lines 1-2 refer to the title of the invention of the Shaver patent, which indicates that the invention is a method and apparatus for detecting memory device types. The Shaver patent discloses in claim 1 a method to determine whether the memory is an extended data output type memory or a fast page mode type memory. Shaver does not appear to ***individually specify at least one of a plurality of banks comprising the memory device having an open row of memory cells that is to be closed***.

Thus, it would not have been obvious to one skilled in the art to come up with the invention covered by scope of claims 14-15 of the instant application after having the Watanbe patent, NEC Manual, and the Shaver Patent. Applicants respectfully request allowance of claims 14-15.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

June 30, 2006
Date

Gregory D. Caldwell
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(viii) Claims appendix.

1. (Original) An apparatus comprising:

a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein only one row of memory cells in each bank may be activated to be open to be accessed at any given time;

control logic coupled to the plurality of banks to control accesses made to each bank in response to commands received from an external device including a precharge command wherein banks of the plurality of banks that are affected by the precharge command are individually specified; and

a plurality of signal lines coupling the control logic to the external device able to support the precharge command using individual ones of a subset of the plurality of signal lines to individually specify the banks of the plurality of banks that are affected by the precharge command.

2. (Original) The apparatus of claim 1, wherein the subset of the plurality of signal lines used to individually specify the banks that are affected by the precharge command is comprised of row address lines also used to transmit a portion of a row address, but not used to transmit a portion of a column address as a result of the use of asymmetric addressing.

3. (Original) The apparatus of claim 2, wherein the use of the row address lines to specify the banks that are affected by the precharge command is enabled through programming a register within the control logic.

4. (Original) The apparatus of claim 3, wherein the plurality of signal lines used to individually specify the banks that are affected by the precharge command is further comprised of bank address lines otherwise used to transmit a portion of a bank address in support of an alternate precharge command, and wherein the programming of a register within the control logic to enable the use the row address lines to individually specify the banks that are affected by the precharge command also results in disabling the use of the bank address lines to support the

alternate precharge command and in enabling the use of the bank address lines to individually specify the banks that are affected by the precharge command.

5. (Original) The apparatus of claim 2, wherein the precharge command is received by the control logic as part of an autoprecharge command embedded within an access command received by the control logic.

6. (Original) A computer system comprising:

a CPU;

a memory device having a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein the memory device is capable of closing open rows in banks individually specified in a precharge command;

a memory bus comprised of a plurality of signal lines coupled to the memory device; and

a memory controller coupled to the CPU and to the memory bus to transmit the precharge command to the memory device across the memory bus wherein banks within the memory device having an open row to be closed in response to the precharge command are individually specified through corresponding individual ones of a subset of the plurality of signal lines of the memory bus.

7. (Original) The computer system of claim 6, in which each of the subset of signal lines used in the precharge command to individually specify a bank in which an open row is to be closed is comprised of row address lines also used to transmit a portion of a row address, but not a portion of a column address, as a result of asymmetric addressing.

8. (Original) The apparatus of claim 7, wherein the memory controller is further comprised of a control register programmable by the CPU to enable the use of the row address lines to individually specify banks having an open row to be closed in the precharge command.

9. (Original) A method comprising:

determining whether or not there is a bank within a plurality of banks within a memory device having an open row that must be closed in preparation for an upcoming access command; and

transmitting a precharge command to the memory device through a subset of signal lines of a memory bus comprised of a plurality of signal lines using individual ones of the subset of signal lines to individually specify at least one bank within the memory device having an open row that is to be closed.

10. (Original) The method of claim 9, wherein determining whether or not there is a bank within a memory device having an open row that must be closed in preparation for an upcoming access command further comprises parsing a queue of upcoming access commands to determine which row must be open in each bank within the plurality of banks within the memory device in preparation for a given upcoming access command within the queue.

11. (Original) The method of claim 9, wherein determining whether or not there is a bank within a memory device having an open row that must be closed in preparation for an upcoming access command further comprises employing at least one prediction algorithm to predict which row must be open in each bank within the plurality of banks within the memory device in preparation for an upcoming predicted access command.

12. (Original) The method of claim 9, further comprising configuring a memory controller to use a plurality of signal lines to individually specify at least one bank within the memory device in which an open row must be closed, as an alternative to using a plurality of bank address lines to transmit a binary code specifying no more than one bank within a memory device in which an open row must be closed.

13. (Original) The method of claim 9, wherein transmitting the precharge command to the memory device further comprises embedding the precharge command in an access command as an autoprecharge command to cause the precharge command to be carried out immediately after the access command is carried out.

14. (Original) A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

carry out a test of a memory device to determine whether or not the memory device supports a precharge command in which individual ones of a subset of signal lines of a memory bus comprised of a plurality of signal lines are used to individually specify at least one of a plurality of banks comprising the memory device having an open row of memory cells that is to be closed; and

program a memory controller coupling the memory device to the CPU to enable the use of a precharge command in which individual ones of the subset of signal lines are used to individually specify at least one of the plurality of banks as an alternative to using a plurality of bank address lines to transmit a binary code across the memory bus specifying only one bank of the plurality of banks having an open row of memory cells that is to be closed in an alternate form of precharge command.

15. (Original) The machine-accessible medium of claim 14, further causing the processor to program the memory controller to enable the use of the bank address lines to comprise at least a portion of the subset of signal lines, and to disable the use of the bank address lines to transmit the binary code specifying only one bank of the plurality of banks.

(ix) Evidence appendix.

None.

(x) Related proceedings appendix.

None.